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| Exp no:3 | Realization of half-adder and full-adder logic circuits |
| Date:  23-09-2021 |

# Aim:

To realize the half-adder and full-adder logic circuits and verify the simulation output with theoretical results.

# Required tools:

Multisim online circuit simulator

# Theory:

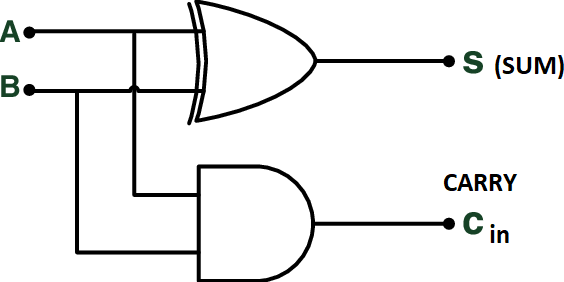
**Half-Adder:**

A combinational logic circuit that performs the addition of two data bits, A and B, is called a half-adder. The addition will result in two output bits; one of which is the sum bit, S, and the other is the carry bit, Cin. The Boolean functions describing the half-adder are:

S = A⊕B

Cin = AB

# Logic Diagram:



**Full-Adder:**

A combinational logic circuit that adds three data bits, A, B, and C is called a full-adder. The Boolean functions describing the full-adder are:

S = A⊕B⊕C

Cin = C(A⊕B)+AB

# Logic Diagram:

**Results:**

Comparison of theoretical results with simulation results for Half Adder

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | Theoretical result according to the expression | | Simulation result | |
| SUM | CARRY | SUM | CARRY |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |

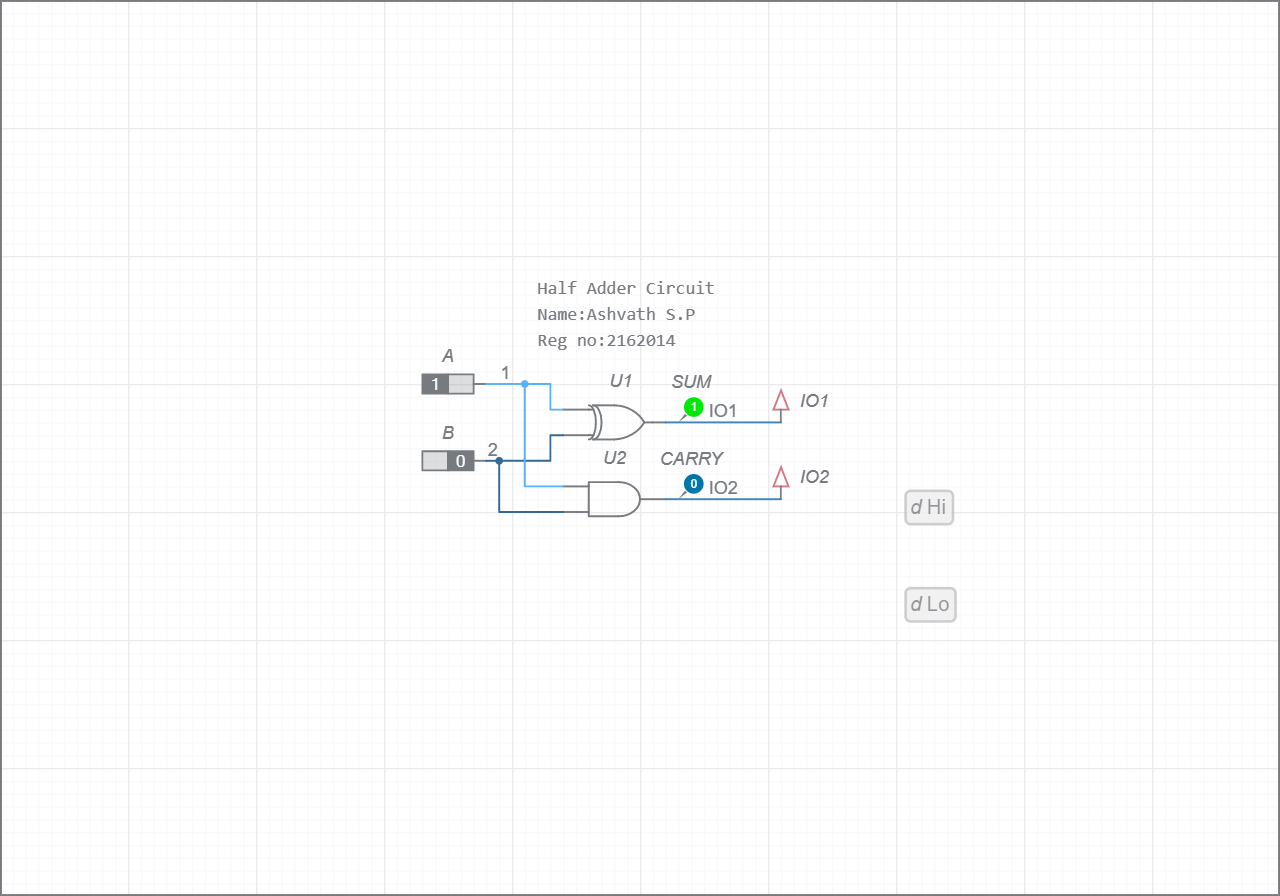


Figure: Logic circuit realization of Half-adder

Comparison of theoretical results with simulation results for Full Adder

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| A | B | C | Theoretical result according to the expression | | Simulation result | |
| SUM | CARRY | SUM | CARRY |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

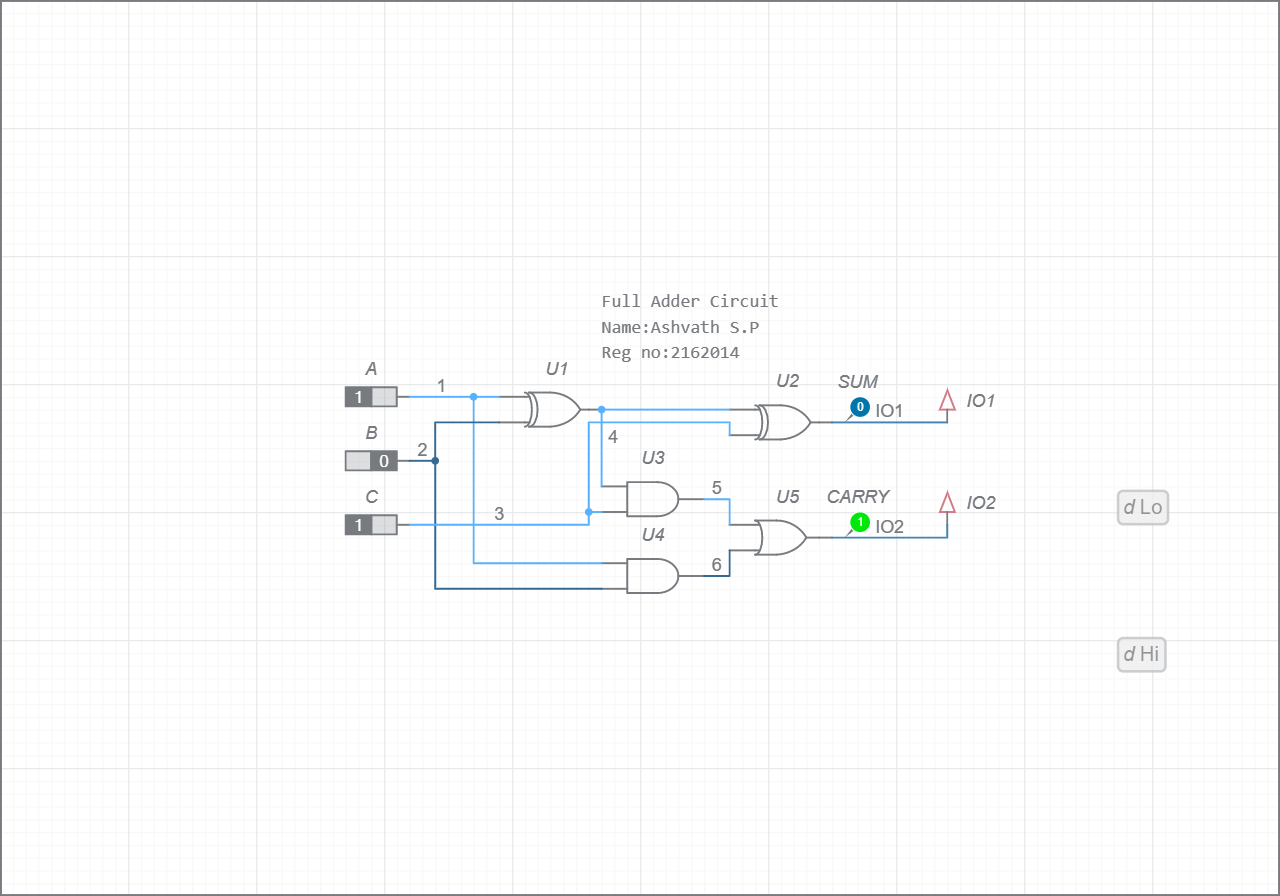
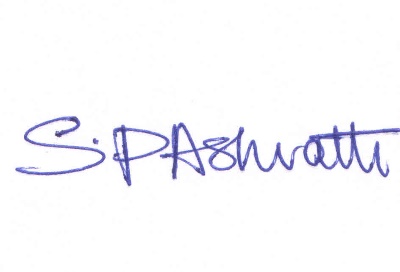


Figure: Logic circuit realization of full-adder

# Inference:

The theoretical and simulation results of the truth table of half-adder and full-adder are in good agreement and verified successfully through multisim online simulator.



Faculty signature:

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Student signature: